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PTO/SB/33 (07-05)
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
1778.0120002 (as amended) (MIPS 0077.20US)

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Signature _____

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Application Number	Filed
09/364,786	July 30, 1999

First Named Inventor
Radhika Thekkath

Art Unit	Examiner
2672	Javid A. Amini

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒ attorney or agent of record.
Registration number 47,415

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Signature

Virgil L. Beaston
Typed or printed name

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Telephone number

5/10/06
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 9876
Thekkath *et al.*	Art Unit: 2672
Appl. No.: 09/364,786	Examiner: D. Pan
Filed: July 30, 1999	Atty. Docket: 1778.0120002 (*as amended*)
For: **Processor Having a Compare Extension of an Instruction Set Architecture**	(MIPS 0077.20US)

Arguments to Accompany the Pre-Appeal Brief Request for Review

Mail Stop AF

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby submit the following Arguments, in five (5) or less total pages, as an attachment to the Pre-Appeal Brief Request for Review (Form PTO/SB/33). A Notice of Appeal is concurrently filed.

Status Of Claims

Claims 1-19 and 40-48 are pending in the application, with 1 and 11 being the independent claims. No claims are presently allowed.

Summary Of Rejections

Claims 1-19 and 40-48 stand rejected under 35 U.S.C. § 112, second paragraph as allegedly be indefinite. According to the Examiner, the limitation "the absolute value of each of the at least one of the plurality of transformed coordinates" renders claims 1 and 11 indefinite, although no reason is given as to why this phrase makes the claims indefinite. The Examiner also alleges that the phrase "a single comparison operation" can not be understood by a person

skilled in relevant art after reading the specification. Finally, the Examiner alleges that there is no antecedent basis for the phrase "the absolute value of each of" recited in claims 1 and 11.

Claims 1-19 and 40-48 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,720,019 ("Koss") in view of U.S. Patent No. 6,169,554 ("Deering") and MIPS R4000 Microprocessor User's Manual ("Heinrick"). In addition, claims 1 and 11 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Koss in view of U.S. Patent No. 6,298,365 ("Dubey") and Heinrick.

Overview Of Invention

Generally speaking, the claimed invention relates to a processor having an expanded instruction set that facilitates 3D graphics processing. One of the instructions of the expanded instruction set is a CABS instruction.

As described in the present application (e.g., beginning on page 88, line 1), in 3-D graphics applications a clip test is performed to determine which primitives, or parts of primitives, will appear in a displayed graphics image. The clip test can be performed using the CABS instruction to compare the absolute values of transformed coordinate values (e.g., x', y', z') for each vertex against the absolute values of the standard viewing planes (e.g., w'). The CABS instruction performs magnitude compares (e.g., $|x'| \leq |w'|$), which replace the conventional two-step inequality evaluations ($x \leq w$ and $x \geq -w$) that are use to implement clip testing in conventional processors.

In paired-single format, the CABS instruction provides the capability for performing two magnitude compares and testing up to four view volume edges in one clock cycle. As described in the present application, in a paired-single format, the CABS instruction can compare the absolute values of a first data set (e.g., x' and y' representing transformed vertex coordinates) with the absolute values of a second data set (e.g., w' and w' representing viewing planes or,

more specifically, two view volume edges of a three-dimensional volume) to clip test four view volume edges in a single operation. (See, e.g., Table 3 on page 90 and the description thereof starting on page 91 of the present application.) This is illustrated by the pseudocode of Table 3. Because the CABS instruction can be executed in a single clock cycle, four view volume edges can be compared in a single cycle.

In accordance with the disclosure of the present application, claim 1 recites:

> 1. In a processor, a method for performing computer graphics view volume clipping comparisons to determine if a vertex is located within a specified view volume, the method comprising:
> transforming a plurality of coordinates representing the vertex into a plurality of transformed coordinates; and
> using a floating point magnitude compare instruction to
> determine an absolute value of at least one of the plurality of transformed coordinates and an absolute value that represents, for each respective at least one transformed coordinate, opposing view volume edges in the specified view volume in a dimension corresponding to the respective at least one transformed coordinate, and
> perform a magnitude comparison between the absolute value of each of the at least one of the plurality of transformed coordinates and the absolute value of the corresponding view volume edges, wherein the magnitude comparison for each transformed coordinate involves a single comparison operation, and wherein comparison results for at least two view volume edges are obtained.

Independent claim 11 recites similar features.

Arguments

The rejection of claims 1-19 and 40-48 under 35 U.S.C. § 112, second paragraph is improper. Given the description contained in the present application, the phrases identified by the Examiner do not render the claims indefinite. There is also proper antecedent basis for the phrase "the absolute value of each of" recited in claims 1 and 11.

The rejection of claims 1-19 and 40-48 under 35 U.S.C. § 103(a) is also improper. Koss relates to a graphics processing circuit for use in a graphics accelerator. (See abstract of Koss.) The graphics accelerator of Koss is not a processor having an expanded instruction set that facilitates 3-D graphics processing. For example, nowhere does Koss disclose or suggest "a floating point magnitude compare instruction" as described and claimed in the present application.

As noted by the Examiner, the graphics accelerator of Koss includes a clipping preprocessor circuit that uses a comparator. The comparator "can be a floating point comparator." (See col. 2, ln. 42 of Koss.) FIG. 4 of Koss actually shows that two floating point comparators are used. As described by Koss at column 8, lines 42-54:

> Each of the floating point comparators 206, 208 compares the two floating point numbers it receives and provides a signal that indicates which one is larger. In particular, the first floating point comparator 206 provides a logic high signal (binary one) on a maximum output line 210 if the value it receives from the vertex coordinate register 202 is higher than the value it receives from the maximum register 200. Conversely, the second floating point comparator 208 provides a logic high signal on a minimum output line 212 if the value it receives from the vertex coordinate register is less than the value it receives from the minimum register 204.

This description in Koss is suggestive of the two-step inequality evaluations ($x \leq w$ and $x \geq -w$) used to implement clip testing in a conventional processor. It does not make obvious the floating point magnitude compare instruction disclosed and claimed in the present application. Koss also states that:

> In order to operate on signed values, the comparators are implemented as magnitude comparators with additional circuitry. In particular, referring also to FIG. 5, the second comparator 208 includes a magnitude comparator 213 that has a first input port operatively connected to the second output bus 203 which is from the output port of the vertex coordinate register 202. The magnitude comparator has a second input port operatively

> connected to the third output bus 205, which is from the output port of the minimum clipping extent register 204.

(See col. 8, ln. 62 - col. 9, ln. 4 of Koss.) This statement by Koss, however, does not change the overall operation of the clipping preprocessor circuit of Koss.

The other references applied by the Examiner do not overcome the deficiencies of Koss.

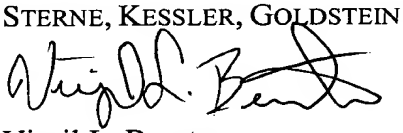
Conclusion

Applicants respectfully submit that claims 1-19 and 40-48 are patentable and, as such, the present application is in condition for allowance. Prompt and favorable consideration of Applicants' Pre-Appeal Brief Request for Review is respectfully requested.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



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Date: May 10, 2006

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